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| **UNIVERSITY OF NIŠ** | | | | | | |
| **Course Unit Descriptor** | | **Faculty** | | | The Faculty of Electrical Engineering | |
| **GENERAL INFORMATION** | | | | | | |
| Study program | | | | Electronics and Microsystems | | |
| Study Module (if applicable) | | | | Electronics | | |
| Course title | | | | System on Chip | | |
| Level of study | | | | ☐Bachelor ☒ Master’s ☐ Doctoral | | |
| Type of course | | | | ☐ Obligatory ☒ Elective | | |
| Semester | | | | ☐ Autumn ☒ Spring | | |
| Year of study | | | | 1 | | |
| Number of ECTS allocated | | | | 5 | | |
| Name of lecturer/lecturers | | | | Damnjanović S. Milunka | | |
| Teaching mode | | | | ☒Lectures ☐Group tutorials ☐ Individual tutorials  ☒Laboratory work ☐ Project work ☐ Seminar  ☐Distance learning ☐ Blended learning ☐ Other | | |
| **PURPOSE AND OVERVIEW (max. 5 sentences)** | | | | | | |
| The aim is to provide students with knowledge about: problems in System on Chip (SoC) design, SoC architectures and SoC design methods. Getting competence in design of specific integrated circuits which contains all elements of one system including appropriate aspects for such complex systems. It is expected for students to learn procedures for designing SoC, and familiarize with associated, specific, problems and methods for manufacturing SoC systems. | | | | | | |
| **SYLLABUS (brief outline and summary of topics, max. 10 sentences)** | | | | | | |
| Design compromises (area, power consumption, speed) from architecture, bus width, noise margin selection point of view. Interconnection models with concentrated and distributed parameters. Signal reflection, delay and loss at signal interconnections. Coupling blocks with different power supply voltage levels. Chip power density distribution. Chip power management. Management of blocks in Idle/standby state. Usage of IP blocks. Macro-cells. Design for testability (DFT). Design for manufacturability (DFM). Guarding rings. Knowledge adopted from theoretical lectures is further improved through skills obtained working in one of the industry CAD/EDA standards, Mentor Graphics ASIC Design Suite, in UNIX/LINUX environment. | | | | | | |
| **LANGUAGE OF INSTRUCTION** | | | | | | |
| ☒Serbian (complete course) ☐ English (complete course) ☐ Other \_\_\_\_\_\_\_\_\_\_\_\_\_ (complete course)  ☐Serbian with English mentoring ☐Serbian with other mentoring \_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | | | |
| **ASSESSMENT METHODS AND CRITERIA** | | | | | | |
| **Pre exam duties** | **Points** | | **Final exam** | | | **points** |
| **Activity during lectures** | **5** | | **Written examination** | | |  |
| **Practical teaching** | **40** | | **Oral examination** | | | **30** |
| **Teaching colloquia** | **25** | | **OVERALL SUM** | | | **100** |
| **\*Final examination mark is formed in accordance with the Institutional documents** | | | | | | |