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| **UNIVERSITY OF NIŠ** | | | | | | |
| **Course Unit Descriptor** | | **Faculty** | | | The Faculty of Electrical Engineering | |
| **GENERAL INFORMATION** | | | | | | |
| Study program | | | | **Electrical Engineering and Computing** | | |
| Study Module (if applicable) | | | | Electronics - Circuits and Systems, Embedded Systems | | |
| Course title | | | | Digital Integrated Circuits Design | | |
| Level of study | | | | ☒Bachelor ☐ Master’s ☐ Doctoral | | |
| Type of course | | | | ☒ Obligatory ☐ Elective | | |
| Semester | | | | ☐ Autumn ☒ Spring | | |
| Year of study | | | | 3 | | |
| Number of ECTS allocated | | | | 6 | | |
| Name of lecturer/lecturers | | | | Petković M. Predrag, Damnjanović S. Milunka | | |
| Teaching mode | | | | ☒Lectures ☐Group tutorials ☐ Individual tutorials  ☒Laboratory work ☐ Project work ☐ Seminar  ☐Distance learning ☐ Blended learning ☐ Other | | |
| **PURPOSE AND OVERVIEW (max. 5 sentences)** | | | | | | |
| *Adoption and systematization of knowledge necessary for full custom digital integrated circuits design and semicustom design based on standard cells (ASIC).* *Student will be competent to: 1. Use CAD tools for digital circuit design (a) based on manual layout drawing of own cell, (b) based on standard cell libraries; (2) Learn LINUX/UNIT operating system; (3) Improve skills to write documentation and to present results.* | | | | | | |
| **SYLLABUS (brief outline and summary of topics, max. 10 sentences)** | | | | | | |
| **Standard and submicron CMOS process. Design rules. Power line tracing. Cases. Floor planning. Full custom design. Transistor sizing. Trade of speed, power consumption and area. Stick diagram. Schematics, simulation, LVS, parameter extraction. ERC. DRC. Cell characterization. Adding a new cell to the library. Standard cell based design. VHDL description. Verification. Automatic synthesis. Delay, power and area forecast. place and route, post-layout verification, Signal integrity. Power line routing. Clock tree. Crosstalk prevention. Antenna effect prevention. Pad ordering. Theoretical knowledge for integrated circuits design students will practice using Mentor Graphics ASIC Design Suite under LINUX/UNIX operating system. Intensive practical laboratory exercises. During the first part of the course students will pass through full custom design flow. They will solve a problem from the practicum. Thereafter, they will get individual project to design a digital module. The second part of the course is organized in the similar way but related to standard cell semi-custom design. Positively marked projects are prerequisite for final exam** | | | | | | |
| **LANGUAGE OF INSTRUCTION** | | | | | | |
| ☒Serbian (complete course) ☐ English (complete course) ☐ Other \_\_\_\_\_\_\_\_\_\_\_\_\_ (complete course)  ☐Serbian with English mentoring ☐Serbian with other mentoring \_\_\_\_\_\_\_\_\_\_\_\_\_\_ | | | | | | |
| **ASSESSMENT METHODS AND CRITERIA** | | | | | | |
| **Pre exam duties** | **Points** | | **Final exam** | | | **points** |
| **Activity during lectures** | **5** | | **Written examination** | | |  |
| **Practical teaching** | **55** | | **Oral examination** | | | **40** |
| **Teaching colloquia** |  | | **OVERALL SUM** | | | **100** |
| **\*Final examination mark is formed in accordance with the Institutional documents** | | | | | | |